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L1	2030	703/2.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/11/14 14:30
L2	260	L1 and (impur\$4 pileup defects diffusion)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/11/14 14:39
L3	82	716/19-21 and (impur\$4 pileup defects diffusion)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/11/14 14:39
L4	724	(716/19-21).ccls. and (impur\$4 pileup defects diffusion)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/11/14 14:39
L5	79	(716/19-21).ccls. and (impur\$4 pileup)	US-PGPUB; USPAT; USOCR	OR	OFF	2006/11/14 14:39
L7	341	716/20.ccls.	US-PGPUB; USPAT	OR	OFF	2006/11/14 14:58
L8	1	716/20.ccls. and (impur\$4 adj pileup)	US-PGPUB; USPAT	OR	OFF	2006/11/14 14:59
L9	7	(model\$4 with semiconductor with (device process) with impurity).clm.	US-PGPUB; USPAT	OR	OFF	2006/11/14 15:03
L10	3	(model\$4 with semiconductor with impurity with distance).clm.	US-PGPUB; USPAT	OR	OFF	2006/11/14 15:08
L11	0	(model\$4 with semiconductor with impurity with lambda).clm.	US-PGPUB; USPAT	OR	OFF	2006/11/14 15:03
L12	1	"6594625".pn.	US-PGPUB; USPAT	OR	OFF	2006/11/14 15:06
L13	0	(model\$4 with semiconductor with impurity with (gate source drain)). clm.	US-PGPUB; USPAT	OR	OFF	2006/11/14 15:08
L14	4	(US-20010025367-\$).did. or (US-5933359-\$ or US-5737250-\$ or US-5502643-\$).did.	US-PGPUB; USPAT	OR	OFF	2006/11/14 15:15
L15	0	(fair with diffusion with model\$4). clm.	US-PGPUB; USPAT	OR	OFF	2006/11/14 15:30
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Title	CATIONIC ELECTRODEPOSITION COATING COMPOSITION	ELECTRODEPOSITION COATING COMPOSITION	CATIONIC ELECTRODEPOSITION COATING COMPOSITION	PROJECTED IMAGE DISPLAYING APPARATUS AND A HAYASHI, HIROKAZU METHOD OF CORRECTING COLOR UNEVENNESS THEREIN	PROFILE EXTRACTION METHOD AND PROFILE EXTRACTION APPARATUS	A METHOD OF FABRICATING A SOI STRUCTURE SEMICONDUCTOR DEVICE	METHOD FOR MODELING DIFFUSION OF IMPURITIES HAYASHI, HIROKAZU In a semiconductor	SOI STRUCTURE SEMICONDUCTOR DEVICE AND A FABRICATION METHOD THEREOF	Method for modeling semiconductor device process	METHOD FOR MODELING SEMICONDUCTOR DEVICE HAYASHI, HIROKAZU AND NETWORK	EVALUATION TEG FOR SEMICONDUCTOR DEVICE AND METHOD OF EVALUATION	ESD protection device modeling method and ESD simulation method	Semiconductor device and method of manufacturing the same HAYASHI, HIROKAZU	Method of evaluating semiconductor device	Semiconductor device and method of producing the same	ELECTRO-STATIC DISCHARGE PROTECTION CIRCUIT AND SEMICONDUCTOR DEVICE HAVING THE SAME	Design and simulation methods for electrostatic protection circuits	Evaluation TEG for semiconductor device and melhod of evaluation	Load driving device	Pile fabric and method for producing the same
Date Filed	6861/00/10	03/03/1989	1661/51/50	10/25/1993	6661/80/70	03/06/2000	02/13/2001	06/27/2001	01/31/2002	09/24/2003	02/19/2004	09/03/2004	11/16/2004	12/03/2004	07/14/2005	03/12/2006	11/22/2005	96/08/2006	9002/20/60	01/01/0001
Status	991	150	150	150	150	150	150	150	80	150	150	41	83	30	30	30	20	20	25	61
Patent#	Not Issued	4904361	1016805	5452019	<u>6581028</u>	6277684	6594625	7129959	Not Issued	6981236	7000201	Not Issued	Not Issued	Not Issued	Not Issued	Not Issued	Not Issued	Not Issued	Not Issued	Not Issued
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of this paper have been tested by extensive simulations [7] and will be published in a future work,
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